CLAIMS

What is claimed is:

- 1 1. An apparatus comprising:
- 2 a die;
- a package coupled to the die; and
- an interposer, coupled to the package and formed from a circuit board
- 5 substrate, by which the apparatus can be electrically coupled to a circuit board.
- 2. An apparatus as recited in claim 1, wherein the interposer comprises a first
- 2 surface, a second surface, and a plurality of conductive paths between the first
- 3 surface and the second surface.
- 1 3. An apparatus as recited in claim 2, wherein the interposer has an edge
- 2 perpendicular to the first surface and the second surface, and wherein each of the
- 3 conductive paths comprises a conductive coating formed in a recessed channel in
- 4 the edge.
- 4. An apparatus as recited in claim 2, wherein each of the conductive paths
- 2 comprises a solid conductive column formed through the substrate.
- 5. An apparatus as recited in claim 4, wherein each of the conductive columns
- 2 has a composition of tin (Sn) and lead (Pb), comprising at least 81% lead (Pb).

- 1 6. An interposer, comprising a circuit board substrate, to couple a
- 2 microelectronic device package to a circuit board.
- 7. An interposer as recited in claim 6, wherein the circuit board substrate has a
- 2 first surface and a second surface parallel to the first surface, the interposer
- 3 further comprising:
- 4 a first plurality of electrical contacts on the first surface;
- a second plurality of electrical contacts on the second surface; and
- 6 a plurality of conductive paths, each from one of the first plurality of
- 7 electrical contacts to one of the second plurality of electrical contacts.
- 8. An interposer as recited in claim 7, wherein the circuit board substrate further
- 2 has an edge perpendicular to the first surface and the second surface, wherein
- 3 each of the conductive paths comprises a conductive coating formed in a
- 4 recessed channel in the edge.
- 9. An interposer as recited in claim 7, wherein each of the conductive paths
- 2 comprises a solid conductive column through the circuit board substrate.
- 1 10. An interposer comprising:
- 2 a substrate having a first surface and a second surface;
- 3 a first plurality of conductive contacts on the first surface to be coupled to
- 4 an electronic component package;

- a second plurality of conductive contacts on the second surface to be coupled to a circuit board; and
- 7 a plurality of conductive paths, each separately connecting one of the first
- 8 plurality of conductive contacts with one of the second plurality of conductive
- 9 contacts.
- 1 11. An interposer as recited in claim 10, wherein the substrate is a circuit board
- 2 substrate.
- 1 12. An interposer as recited in claim 10, wherein each of the conductive paths
- 2 comprises a conductive coating formed in a recessed channel in an edge of the
- 3 substrate, the edge perpendicular to the first surface and the second surface.
- 1 13. An interposer as recited in claim 12, wherein each of the recessed channels is
- 2 a portion of a cylindrical through hole.
- 1 14. A device to couple an electronic component package to a circuit board, the
- 2 device comprising a plurality of interposers coupled to each other, each being an
- 3 interposer as recited in claim 13.
- 1 15. An interposer as recited in claim 14, wherein the plurality of interposers are
- 2 coupled together to form an array of conductive paths to couple the electronic
- 3 component package to the circuit board.

- 16. An interposer as recited in claim 10, wherein each of the conductive paths 1 comprises a solid conductive column through the substrate from the first surface 2 to the second surface. 3 17. An interposer as recited in claim 16, wherein each of the conductive columns 1 is an alloy of tin (Sn) and lead (Pb), comprising at least 81% lead (Pb). 2 18. An electronic apparatus comprising: 1 a die having a plurality of electronic circuits formed thereon; 2 a package substrate having a first surface coupled to the die and a second 3 surface; 4 a circuit board; and 5 an interposer coupled between the second surface of the package substrate 6 and the circuit board, the interposer comprising 7 a circuit board substrate having a first surface and a second surface, 8 a first plurality of conductive contacts disposed on the first surface 9 to be coupled to an electronic component package, 10
- a second plurality of conductive contacts disposed on the second surface to be coupled to a circuit board, and
- a plurality of conductive paths, each separately connecting one of the first plurality of conductive contacts with one of the second plurality of conductive contacts.

- 1 19. An electronic apparatus as recited in claim 18, wherein each of the
- 2 conductive paths comprises a conductive coating formed in a recessed channel in
- 3 an edge of the circuit board substrate, the edge perpendicular to the first surface
- 4 and the second surface.
- 1 20. An electronic apparatus as recited in claim 19, wherein each of the recessed
- 2 channels is a portion of a cylindrical through hole.
- 1 21. An electronic apparatus as recited in claim 18, wherein each of the
- 2 conductive paths comprises a solid conductive column through the circuit board
- 3 substrate from the first surface to the second surface.
- 1 22. An electronic apparatus as recited in claim 21, wherein each of the
- 2 conductive columns has a composition of tin (Sn) and lead (Pb), comprising at
- 3 least 81% lead (Pb).
- 1 23. A method of coupling an electronic circuit package to a circuit board, the
- 2 method comprising:
- 3 coupling a plurality of electrical contacts on a first surface of an interposer
- 4 to the electronic circuit package, the interposer formed from a circuit board
- 5 substrate having the first surface, a second surface, and a plurality of conductive
- 6 paths from the first surface to the second surface; and
- 7 coupling a plurality of electrical contacts on the second surface to the

- 8 circuit board.
- 1 24. A method as recited in claim 23, wherein the electronic circuit package
- 2 includes a semiconductor die.
- 1 25. A method as recited in claim 24, wherein the circuit board is a motherboard.
- 1 26. An interposer comprising:
- a circuit board substrate member having a first surface and a second
- 3 surface parallel to each other, the substrate further having an edge perpendicular
- 4 to the first surface and the second surface;
- a first plurality of conductive contact pads on the first surface;
- a second plurality of conductive contact pads on the second surface; and
- 7 a plurality of recessed channels in the edge of the substrate member,
- 8 extending from the first surface to the second surface, each of the recessed
- 9 channels having a conductive material therein to form a conductive path
- 10 between one of the first plurality of contact pads and one of the second plurality
- 11 of contact pads.
- 1 27. An interposer as recited in claim 26, wherein the recessed channels are
- 2 concave.
- 1 28. An interposer as recited in claim 27, wherein each of the recessed channels is
- 2 a portion of a though hole.

- 1 29. An interposer as recited in claim 26, further comprising a first plurality of
- 2 grooves in the first surface between the contact pads on the first surface.
- 1 30. An interposer as recited in claim 29, further comprising a second plurality of
- 2 grooves in the second surface between the contact pads on the second surface.
- 1 31. A device to couple an electronic component package to a circuit board, the
- 2 device comprising a plurality of interposers coupled to each other, each being an
- 3 interposer as recited in claim 26.
- 1 32. An interposer as recited in claim 31, wherein the plurality of interposers are
- 2 coupled together to form an array of conductive paths to couple the electronic
- 3 component package to the circuit board.
- 1 33. A method comprising:
- 2 creating a plurality of rows of via holes through a circuit board substrate
- 3 from a first surface of the substrate to a second surface of the substrate, the first
- 4 surface and the second surface being coated with a conductive material;
- forming a conductive layer in each of the via holes to provide a
- 6 conduction path through each of the via holes from the conductive material on
- 7 the first surface to the conductive material on the second surface;
- 8 selectively removing some of the conductive material from the first
- 9 surface and the second surface to form a plurality of traces on the first surface

- and the second surface, each trace in electrical contact with the conductive layer
 in at least one of the via holes; and
- severing the substrate to produce a plurality of individual substrate members, by cutting the substrate through the middle of the via holes in each row of via holes and between each row of via holes along a particular axis.
 - 1 34. A method as recited in claim 33, further comprising forming grooves in the
- 2 first surface and the second surface of the substrate between the via holes.
- 1 35. A method as recited in claim 33, wherein the conductive coating is a surface
- 2 layer applied in each of the via holes.
- 1 36. A method as recited in claim 33, wherein said severing comprises severing
- the substrate to produce a plurality of elongate individual substrate members.
- 1 37. A method as recited in claim 36, further comprising affixing two or more of
- 2 the plurality of individual substrate members together to form a substantially
- 3 planar array.
- 1 38. A method as recited in claim 33, further comprising coupling the interposer
- 2 between an electronic component package and a circuit board.
- 1 39. A method as recited in claim 38, wherein the electronic component package
- 2 includes a semiconductor die, and wherein the circuit board is a motherboard.

- 1 40. An interposer comprising:
- 2 a circuit board substrate having a first surface and a second surface
- 3 parallel to each other;
- a first plurality of conductive contact pads on the first surface;
- a second plurality of conductive contact pads on the second surface; and
- a plurality of solid conductive columns through the substrate
- 7 perpendicular to the first surface and the second surface, each in electrical
- 8 contact with one of the first plurality of contact pads and one of the second
- 9 plurality of contact pads.
- 1 41. An interposer as recited in claim 40, further comprising a first plurality of
- 2 grooves in the first surface between the conductive columns on the first surface.
- 1 42. An interposer as recited in claim 41, further comprising a second plurality of
- 2 grooves in the second surface between the conductive columns on the second
- 3 surface.
- 1 43. An interposer as recited in claim 40, wherein the conductive material is an
- 2 alloy of tin (Sn) and lead (Pb), comprising at least 81% lead (Pb).
- 1 44. A method of manufacturing an interposer, the method comprising:
- 2 creating a plurality of via holes through a circuit board substrate from a
- 3 first surface of the substrate to a second surface of the substrate, the first surface

- 4 and the second surface being coated with a conductive material; and
- 5 creating a solid conductive column though each of the via holes, the
- 6 conductive column forming an electrical path from the first surface to the second
- 7 surface.
- 1 45. A method as recited in claim 44, further comprising selectively removing
- 2 some of the conductive material from the first surface and the second surface to
- 3 form a plurality of traces on the first surface and the second surface, each trace in
- 4 electrical contact with the conductive column of one of the via holes.
- 1 46. A method as recited in claim 44, further comprising forming grooves in the
- 2 first surface and the second surface of the substrate between the via holes.
- 47. A method as recited in claim 44, further comprising coupling the interposer
- 2 between an electronic component package and a circuit board.
- 1 48. A method as recited in claim 47, wherein the electronic component package
- 2 includes a semiconductor die and the circuit board is a motherboard.
- 1 49. A method as recited in claim 44, wherein each of the conductive columns has
- 2 a composition of tin (Sn) and lead (Pb), comprising at least 81% lead (Pb).